AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraphs in the specification to correct typographical errors.

Please replace the paragraph on page 3, beginning on line 18 (paragraph [0011] of the published application) with the following:

In any methodology for designing ICs based on predefined component blocks, one of the first steps is to specify, as a starting point, the component blocks that will be used as the foundation of the design. One such component block that is identified at this stage is the foundation block, a block that typically comprises a processor, some memory and a communication block. The communication block has the primary purpose of transferring data from one place to another, ~~an~~and in the context of IC design includes a bus connected to multiple I/O ports. The foundation block often manages the communication between most if not all of the other component blocks to be used in the IC. Because it includes a communication block, the foundation block typically includes on its edges a large number of ports, of which some are initiators and others are targets. Because of the requirements of standard protocols such as the VCI protocol, the type of interface at a particular location on the edge of a foundation block must be predefined. Thus, characterizing the foundation block that is to be used for a given IC typically requires specifying a bus and the number, locations and types of ports on the edges of the block. For example, one common layout of ports for a foundation block is to position them evenly around the foundation block to provide for floor-planning flexibility

Please replace the paragraph on page 6, beginning on line 5 (paragraph [0017] of the published application) with the following:

The present invention, in one aspect, provides a systems and methods for designing an integrated circuit and for creating and using an androgynous interface between electronic components of an integrated circuit.

Please replace the paragraph on page 7, beginning on line 15 (paragraph [0023] of the published application) with the following:

In yet another aspect, a method of designing an integrated circuit includes several steps. In one step, a foundation block for the integrated circuit is specified, including specifying the locations of multiple androgynous interfaces in the integrated circuit. In another step, one or more component blocks ~~to comprise~~ comprising the integrated circuit are identified. In another step, the component blocks to form a layout of the integrated circuit are positioned in a manner that minimizes connection distances between functional blocks and between functional blocks and the androgynous interfaces of the foundation block. In another step, the androgynous interfaces are set to perform as targets or initiators based on the layout.

Please replace the paragraph on page 14, beginning on line 1 (paragraph [0044] of the published application) with the following:

In the next step 303, a form of logic synthesis is performed, where in one preferred embodiment, the functional description of the connections between the components is converted into a specific connection implementation which may be stored in the form of a netlist file 304. As part of this compile process 303, the component library 306 is generally referenced, which stores information concerning the androgynous interface, and the characteristics of the components which are needed in order to determine their functional connectivity. The netlist file 304, as previously noted, generally identifies the component blocks from the library 306, and describes the specific component-to-component connectivity.

Please replace the paragraph on page 15, beginning on line 10 (paragraph [0048] of the published application) with the following:

FIG. 4 details a preferred method 400 for designing an IC such that the layout is optimized without having to adhere to specifications regarding ~~the~~ whether a port is a target or an initiator. In a particular embodiment, the ports that are unspecified, as to being targets or initiators, are on the IC's foundation block, which includes a processor, memory, and a

communication block that specifies a bus and a plurality of ports that will in operation perform as either targets or initiators. In a first step 402, the communication block (or the complete foundation block) is specified. This communication block may be extracted from the component library as part of a logic synthesis operation or may be originally designed. The communication block preferably is specified with a particular bus configuration and footprint on the IC chip. The communication block is further described by a fixed number of ports and particular locations around the block. Each port is defined to be androgynous such that at this stage of design, it can be later adapted or bound to perform as a target or an initiator.

Please replace the paragraph on page 20, beginning on line 8 (paragraph [0062] of the published application) with the following:

In the BVCI, the Error signal does not exist, but is specified for the androgynous VC interface. Furthermore, the Wrap, Const, Contig signals in BVCI are assumed to be part of the Cmd signal in the androgynous VC interface depicted in FIG. 5. Additional return signals are defined for androgynous interface, such as Cmd, Clen, Cfix, which do not have return signals in the BVCI. However, the specification of these signals enables both sides of the androgynous VC interface to look the same, and therefore creates an androgynous interface that is symmetric. The target and initiator sides of the interface have the same number of pins, the same connections, and pin designations.